layer to form respective first and a second junctions therewith. Further, the integrated structure also includes an isolating element positioned between the first and the second regions and extending from the surface of the epitaxial layer at least as far as a top surface of the substrate. The isolating element partially surrounds at least one of the first and second regions. Furthermore, the isolating element also terminates above a bottom surface of the substrate.

Independent Claims 12 and 22 are directed to related integrated structures which similarly recite that the isolating elements thereof terminate above a lower surface of the substrate. Because of the isolating element and relative conductivities of the various elements recited in these claims, an injection of current through the epitaxial layer from the first to the second region is advantageously reduced when the first junction is directly biased, for example.

II. The Claims Are Patentable

A. Chang et al.

The Examiner rejected independent Claims 12, 17, and 22 over Chang et al. As noted in the Amendment filed August 22, 2002, Chang et al. discloses an integrated circuit chip which has full trench dielectric isolation of each portion of the chip. Initially the chip substrate **10** is of conventional thickness (e.g., 500 μm) and has semiconductor devices formed therein. After etching trenches **72** in the substrate **10** and filling them with dielectric material (see FIGS. 1 and 3 of Chang et al.), a heat sink cap **100** is attached to the passivation layer **96** on the front side surface of the substrate **10**. The backside surface of the substrate **10** is removed (by grinding or chemical mechanical polishing (CMP)) to expose the bottom portion of the trenches **72** (see FIG. 7 of

Chang et al). Thus, the dielectric isolation material in the trenches extends completely through the substrate **10**. This is done to fully isolate each portion of the die and eliminate mechanical stresses at the trench **72** bottoms. Thereafter, drain or collector electrical contacts **104a**, **104b** are provided on the substrate **10** backside surface.

In contrast to the integrated circuit chip of Chang et al., the isolating element recited in each of the above noted independent claims terminates above the bottom surface of the substrate. That is, the present invention achieves desired isolation based upon the isolation element and the relative conductivities of the various elements (see, e.g., page 9 of the originally filed specification). However, Chang et al. requires that the dielectric material extend completely through the substrate to achieve the desired isolation properties. To do so, the substrate thereof has to be reduced in thickness from 500 µm to about 5 to 100 µm via CMP, etc. (see col. 6, lines 5-24 of Chang et al.), a costly and time consuming procedure. Yet, the integrated structure of the present invention provides desired isolation without such additional processing.

In response to the above argument, the Examiner correctly acknowledges that "Chang et al. admittedly teaches specifically against trenches that do not terminate above a bottom surface of the substrate." Final Office Action, page 2. Nonetheless, the Examiner contends that Chang et al. does in fact teach "other embodiments" in which this is not the case. As support for this contention, the Examiner points to FIGS. 13 and 14 of Chang et al.

It is respectfully submitted that the Examiner once again has mischaracterized Chang et al. By way of background, the Examiner's rejection set forth in the Office Action of April 22, 2002 relied upon a first embodiment illustrated in

FIGS. 1-12 of Chang et al. for a surface mount integrated circuit chip (see col. 4, lines 4-6). Indeed, FIGS. 1-12 illustrate the successive steps in the method for making the surface mount integrated circuit chip. As noted above, FIG. 7 illustrates the step in which the substrate backside surface is removed to expose the bottom portion of the trenches **72** so that the dielectric isolation material in the trenches extends completely through the substrate **10**.

Chang et al. also discloses a second embodiment in which the same process is used to make a flip chip integrated circuit, the steps of which are illustrated in FIGS. 13-17. Chang et al. first notes that the steps illustrated in FIGS. 1-5 for the surface mount embodiment are identical for the flip chip embodiment (see col. 7, lines 39-41). The steps illustrated in FIGS. 13-14 merely illustrate certain alterations in the fabrication process which result from the two different chip configurations. For example, Chang et al. states in col. 7, lines 43-49 that "[t]he structure of FIG. 13 is identical to that of FIG. 5, except that in FIG. 13 the next step is that passivation layer **160** (which is similar in material and thickness to passivation layer **96** in FIG. 6) is masked using a mask layer (not shown) which is patterned, with subsequent etching to define contact openings **164a**, **164b**, **164c** therethrough." FIG. 14 then simply illustrates the addition of a heat sink cap **172** and associated interconnect structures **176a**-**176c**.

Then, in FIG. 15, which the Examiner fails to mention in the Final Office Action, Chang et al. illustrates the exact same step of removing the backside of the substrate **10** so that the insulated trenches **72a**-**72e** are completely exposed. The text of Chang et al. clearly illustrates that this is the case:

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> Next in FIG. 15, (similar to FIG. 7) the backside surface of substrate **10** is polished or etched away to expose the lower portions of dielectrically insulated trenches **72a, ... , 72e**. Again, the total thickness of substrate **10** and epitaxial layer **20** is minimized by this removing step to that needed for proper electrical functioning. Next in FIG. 16, backside contacts **178a, 178b** are formed, similar to contacts **104a, 104b** in FIG. 8. (Col. 8, lines 22-29) (emphasis added).

Thus, Chang et al. explicitly teaches in every embodiment thereof that the isolation trenches must not terminate above a bottom surface of the substrate, but rather extend all the way through to the back side of the substrate.

As such, Chang et al. fails to teach or fairly suggest all of the elements recited in each of the above noted independent claims, and the rejection of these claims based upon Chang et al. should be withdrawn. Again, Chang et al. in fact teaches those of skill in the art away from making an integrated structure with dielectric-filled trenches that terminate above the bottom surface of the substrate. That is, Chang et al. teaches that such trenches must extend completely through the substrate to achieve "full electrical isolation," which is the stated purpose of the patent (see col. 7, lines 19-21). To have done otherwise would have destroyed the intended purpose of the integrated circuits of Chang et al., and thus rendered them unsatisfactory for their intended purpose.

B. Wada and Endo et al.

The Examiner also rejected independent Claim 12 based upon Wada in view of Endo et al. Wada is directed to a semiconductor device which includes a substrate **1**, an epitaxial layer **2** on the substrate, and diffused regions **14** and **15** in the epitaxial layer which serve as a drain and

source of a DRAM memory cell. Wada also discloses trench structures **31** formed in trenches **4a**, **4b** which are positioned between adjacent DRAM cells. Indeed, Wada notes that these trench structures **31** are for "dielectrically isolating memory cells adjacent to each other in a direction parallel to the word lines." Col. 5, lines 32-34. The trench structures **31** are filled with an insulator **5** (see col. 5, line 30).

The Examiner contends that the trench structure **31** of Wada is equivalent to the isolating element recited in Claim 12, with the exception that Wada does not disclose that the trench structure includes polycrystalline silicon spaced apart from the epitaxial layer by a dielectric material. Nonetheless, the Examiner notes that Endo et al. is directed to a semiconductor device which includes trenches including a dielectric material **46** lining the trench and polycrystalline silicon **47** filling the inner portion of the trench, and he contends that it would have been obvious to combine these teachings to produce the claimed invention.

Again, it is respectfully submitted that the Examiner has mischaracterized Wada. Indeed, as clearly stated in the above-quoted text from Wada, the trench structures **31** are for dielectrically isolating <u>adjacent memory cells</u> from one another, NOT for isolating the source and drain regions **14** and **15** from one another. The trench structures **31** are not located between the source and drain regions **14** and **15**, and they will therefore not reduce an injection of current though the epitaxial region between the regions **14** and **15** when one of these regions is directly biased. As such, even assuming *arguendo* that the combination of Wada and Endo et al. is proper, the proposed combination still fails to teach or fairly suggest each of the elements recited in Claim 12, and the rejection of Claim 12 based thereon cannot stand for this reason alone.

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Accordingly, it is submitted that independent Claims 12, 17, and 22 are patentable over the prior art. Their respective dependent claims, which recite yet further distinguishing features, are also patentable over the prior art and require no further discussion herein.

CONCLUSIONS

In view of the arguments presented above, it is submitted that all of the claims are patentable. Accordingly, a Notice of Allowance is respectfully requested in due course. Should any minor informalities need to be addressed, the Examiner is encouraged to contact the undersigned attorney at the telephone number listed below.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: DIRECTOR, U.S. PATENT AND TRADEMARK OFFICE, BOX AF, WASHINGTON, D.C. 20231, on this 21st day of January, 2003.

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